

Fig 1

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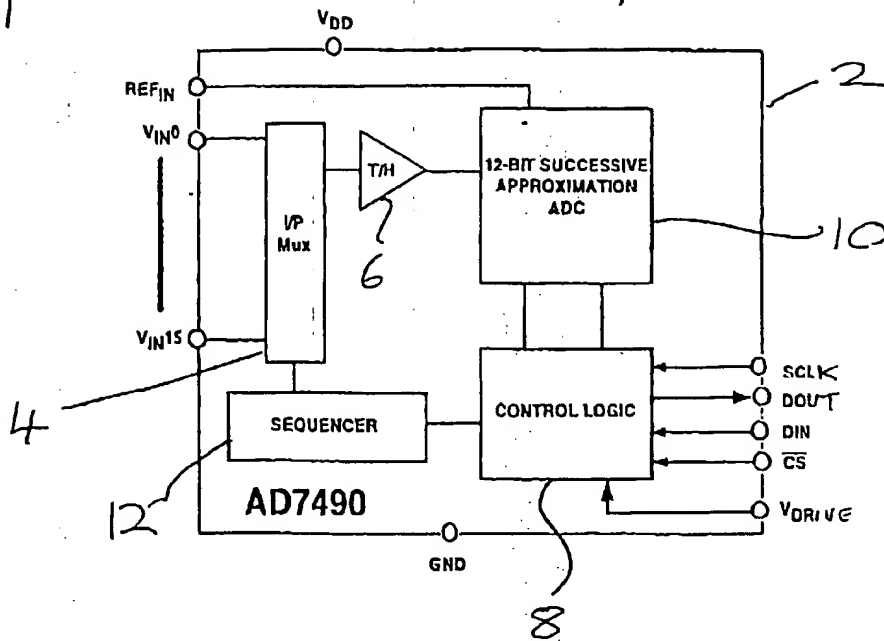
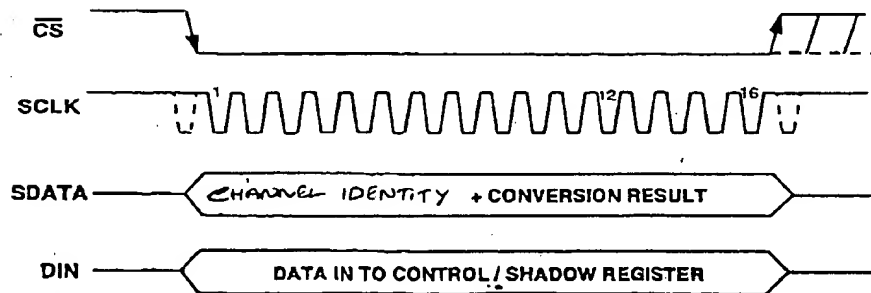
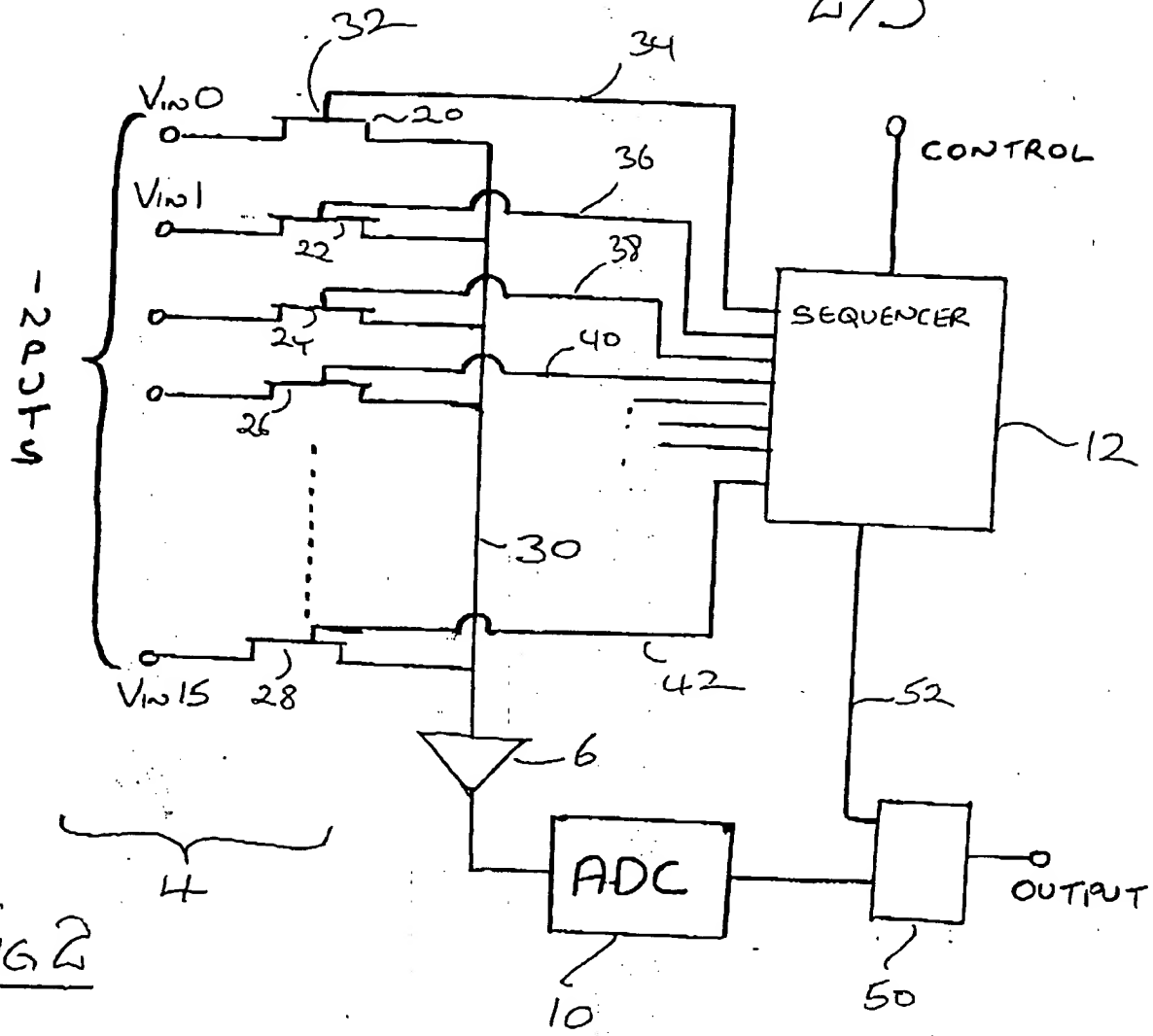


Fig 8



CONTROL REGISTER DATA IS LOADED IN ON FIRST 12 SCLK CYCLES.
SHADOW REGISTER DATA IS LOADED IN ON FIRST 16 SCLK CYCLES



MSB

WRITE	SEQ	ADD3	ADD2	ADD1	ADD0	PM1	PM0	SHADOW	WEAK/TRI	RANGE	CODING
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LSB

FIG 6

MSB

V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}	V_{IN5}	V_{IN6}	V_{IN7}	V_{IN8}	V_{IN9}	V_{IN10}	V_{IN11}	V_{IN12}	V_{IN13}	V_{IN14}	V_{IN15}
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LSB

S0 S1 S2 S3 S4 S15

FIG 7

10311 16423663

Fig 4

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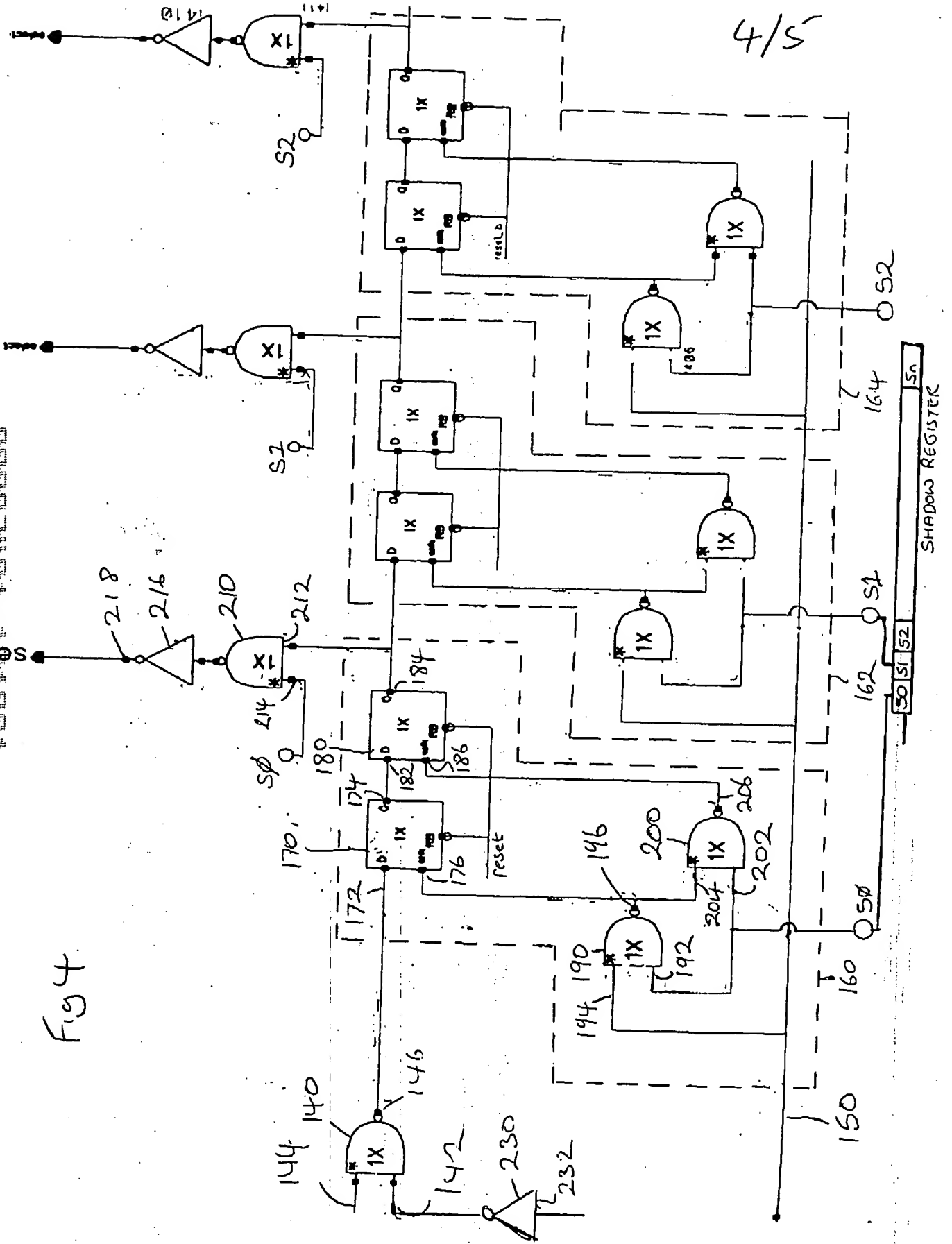


Fig 5

